Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-11 (Canceled)

Claim 12 (Currently amended): A method for fabricating a semiconductor device comprising:

providing a substrate which has a chip region and a pad region which is [[in the]] at a periphery of the chip region;

placing plural conductive pads on the pad region;

mounting a semiconductor chip on the chip region, wherein the semiconductor chip includes a plurality of electrode pads which are formed thereon;

connecting conductive lines between the electrode pads and the conductive pads;

forming a first wall in the pad region;

forming a second wall on the semiconductor chip so as to face [[to]] the first wall, such that the conductive lines are arranged between the first and second walls; and

supplying an encapsulating material into a space between the first and second walls so as to encapsulate the conductive lines.

Claim 13 (Original): The method according to claim 12, further comprising shaving a top surface of the second wall after supplying the encapsulating material.

Claim 14 (Original): The method according to claim 12, wherein a concave portion is located in the chip portion, and wherein the semiconductor chip is mounted in the concave portion.

Claim 15 (Currently amended): A method for fabricating a semiconductor device comprising:

providing a substrate which has a chip region and a pad region which is [[in the]] at a periphery of the chip region;

placing plural conductive pads on the pad region;

mounting a semiconductor chip on the chip region, wherein the semiconductor chip includes a plurality of electrode pads which are formed thereon;

connecting the electrode pads with the conductive pads by conductive lines;

forming a first wall in the pad region;

placing a cover above the chip region, wherein the cover includes an open portion for introduction of an encapsulating material; and

introducing the encapsulating material into a space between the cover and the chip region through the open portion so as to encapsulate a surface of the semiconductor chip and the conductive lines.

Claim 16 (Currently amended): The method according to claim 15, wherein the cover has [[a]] an upper surface and a lower surface which faces [[to]] the chip region, wherein a release agent is formed on the lower surface before introducing the encapsulating material.

Claim 17 (Currently amended): The method according to claim 15, wherein the cover is a lattice structure, and wherein grids of the cover [[is]] are placed so as to extend over [[to]] an upper surface of the conductive lines.

Claim 18 (Original): The method according to claim 15, wherein the first wall surrounds the chip region, and wherein an area of the cover is less than an area which is surrounded by the first wall.

Claim 19 (Currently amended): The method according to claim 15, wherein the cover includes a second open portion through which ~~exhausts~~ a gas in a space between the chip region and the cover is exhausted while introducing the encapsulating material.

Claim 20 (Currently amended): The method according to claim 19 [[15]], wherein the gas is exhausted by an aspirator.

Claim 21 (New): A method for fabricating a semiconductor device comprising:

providing a substrate which has a chip region and a pad region which is at a periphery of the chip region;

providing a conductive pad on the pad region;

mounting a semiconductor chip on the chip region, wherein the semiconductor chip includes an electrode pad thereon;

forming a first wall in the pad region;

forming a second wall on the semiconductor chip, the second wall being formed of a resin and facing toward the first wall;

connecting a conductive line between the electrode pad and the conductive pad, the conductive line being arranged between the first wall and the second wall; and

supplying an encapsulating material between the first and second walls to encapsulate the conductive line,

wherein an upper surface of the first wall and an upper surface of the second wall are set at a substantially same level.

Claim 22 (New): A method for fabricating a semiconductor device comprising:

providing a substrate having a conductive pad affixed thereto;

mounting a semiconductor chip on the substrate, the semiconductor chip having an electrode pad formed on a surface thereof;

forming a first wall on a surface of the substrate, wherein the conductive pad is affixed to a surface of the substrate between the first wall and the semiconductor chip;

connecting a conductive line between the conductive pad and the electrode pad;

forming a second wall on the semiconductor chip; and

supplying an encapsulating material between and in direct contact with the first and second walls to be contained by the first and second walls, to encapsulate the electrode pad and the conductive line,

wherein an upper surface of the first wall and an upper surface of the second wall are at a substantially same level.

Claim 23 (New): The method for fabricating a semiconductor device of claim 22, wherein said forming the second wall comprises providing the second wall so as to have a first surface mounted on the semiconductor chip and a second surface opposite the first surface, the second surface being longer than the first surface so that the second wall overlaps above the conductive line and the electrode pad.

Claim 24 (New): The method for fabricating a semiconductor chip of claim 22, wherein the substrate includes a concave portion having a central region and a peripheral region surrounding the central region, said mounting a semiconductor chip comprises arranging the semiconductor chip in the central region of the concave portion, and said supplying an encapsulating material comprises filling the peripheral region of the concave portion with the encapsulating material.

Claim 25 (New): The method for fabricating a semiconductor chip of claim 22, wherein the encapsulating material is a resin.

Claim 26 (New): The method for fabricating a semiconductor chip of claim 22, wherein the second wall is formed of resin.